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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,038	YEH, TSE-YU	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,10-12,14,15,17,18,23-25 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-5, 10-12, 14-15, 17-18, 23-25, and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-5, 10-12, 14-15, 17-18, 23-25, and 27 have been considered. Claims 1, 14, and 27 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 29 August 2005; Extension of Time for 2 Months as received on 29 August 2005; and Amendment as received on 29 August 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, 14-15, 17-18, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riordan et al., U.S. Patent Number 5,027,270 (herein referred to as Riordan) in view of Eisen et al., U.S. Patent Number 5,897,651 (herein referred to as Eisen) and further in view of Merchant et al., U.S. Patent Number 6,665,792 (herein referred to as Merchant).

5. Referring to claim 1, Riordan has taught a processor comprising:

a. A control circuit, wherein the control circuit is configured to detect a replay of an instruction in a load/store pipeline due to a load miss (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1), and

b. Wherein the control circuit is configured to enter into a stall state and inhibit issuance of instructions to the load/store pipeline until fill data in response to the load miss is returned for loading (Riordan column 3, lines 11-38),

c. The control circuit to compare the stored tag to a fill tag that is sent to the control circuit when fill data is returned (Riordan column 3, lines 11-38). In regards to Riordan, the stored tag is the address of the instruction and the fill tag is the TAG field.

d. In which when the tag and the fill tag match, the control circuit is to exit the stall state to start issuing instructions from the queue to the pipelines (Riordan column 3, line 52 to column 4, line 2).

6. Riordan has not explicitly taught

a. A queue configured to store one or more instructions to be issued; and

b. A control circuit coupled to the queue

c. The control circuit further includes a storage device to store a miss tag corresponding to the load miss

7. However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Eisen has taught

a. A queue configured to store one or more instructions to be issued (Eisen column 2, lines 10-14; column 5, lines 37; and Figure 3); and

b. A control circuit coupled to the queue (Eisen column 5, lines 26-38 and Figure 3);

c. The control circuit further includes a storage device to store a miss tag corresponding to the load miss (Eisen column 5, lines 26-38 and 49-60; column 6, lines 19-32; and Figure 3).

8. In regards to Eisen, the tag bits set within the sequencer are set when a cache miss occurs, thereby making it a miss tag. A person of ordinary skill in the art at the time the invention was made, and as taught by Eisen, would have recognized that the tags allow a system to start fetching instructions from the cache before the entire block has been written (Eisen column 4, lines 23-40), thereby reducing fetch delays and improving cache memory management and system performance (Eisen column 4, lines 14-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the tags of Eisen in the device of Riordan to improve cache memory management and system performance.

9. In addition, Riordan has not taught inhibiting issuance of instructions to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss. Merchant has taught inhibiting issuance of instructions to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss (Merchant column 1, lines 26-50 and column 2, line 42 to column 3, line 7). In regards to Merchant, by not scheduling dependent instructions to execute when an instruction is dependent upon a stalled instruction, the system is effectively inhibiting the instruction from executing. A person of ordinary skill in the art at the time the invention was made, and as recognized by Merchant, would have recognized that out-of-order execution and replaying cache miss load instructions reduces overall latency (Merchant column

1, lines 39-40) and prevents incorrect data from polluting the cache system and wasting bus resources (Merchant column 3, lines 1-7), thereby increasing performance (Merchant column 1, lines 39-40) and ensuring correct data is executed on. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order execution and replay of Merchant in the device of Riordan to increase performance and ensuring correct data.

10. Referring to claim 2, Riordan in view of Eisen and in further view of Merchant has taught wherein the control circuit is configured to inhibit issuance of the instructions until fill data is provided to a data cache of the processor (Riordan column 3, lines 11-38).

11. Referring to claims 4 and 5, Riordan has taught

a. Wherein the control circuit further includes a comparator coupled to the storage device to compare the tag to the fill tag to determine if the fill data being returned corresponds to the load miss (Applicant's claim 4) (Riordan column 3, lines 11-38). In regards to Riordan, the stored tag is the address of the instruction and the fill tag is the TAG field.

b. Wherein a load miss may be present in which comparison of the tag and the fill tag identifies fill data to its corresponding load miss (Applicant's claim 5) (Riordan column 3, lines 11-38).

12. Riordan has not explicitly taught a miss tag (Applicant's claims 4 and 5). However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Eisen has taught a miss tag (Applicant's claims 3

and 4) (Eisen column 5, lines 26-38 and 49-60; column 6, lines 19-32; and Figure 3). In regards to Eisen, the tag bits set within the sequencer are set when a cache miss occurs, thereby making it a miss tag. A person of ordinary skill in the art at the time the invention was made, and as taught by Eisen, would have recognized that the tags allow a system to start fetching instructions from the cache before the entire block has been written (Eisen column 4, lines 23-40), thereby reducing fetch delays and improving cache memory management and system performance (Eisen column 4, lines 14-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the tags of Eisen in the device of Riordan to improve cache memory management and system performance.

13. Referring to claim 14, Riordan has taught a method comprising:

a. Detecting a replay of a first instruction due to a dependency on a load miss in a load/store pipeline of a processor (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1);

b. Inhibiting issuance of one or more instructions from a queue to the load/store pipeline responsive to detecting the replay by entering a stall state (Riordan column 3, lines 11-38);

c. Generating a fill tag when fill data corresponding to the load miss is returned (Riordan column 3, lines 11-38). In regards to Riordan, the stored tag is the address of the instruction and the fill tag is the TAG field.

d. Comparing the fill tag to the tag to identify when fill data corresponding to the load miss is being returned (Riordan column 3, lines 11-38). In regards to

Riordan, the stored tag is the address of the instruction and the fill tag is the TAG field.

e. Exiting the stall state to allow one or more instructions to issue after comparing the fill tag and the tag results in a match (Riordan column 3, line 52 to column 4, line 2).

14. Riordan has not explicitly taught storing a miss tag corresponding to the load miss in response to detecting the replay. However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Eisen has taught storing a miss tag corresponding to the load miss in response to detecting the replay (Eisen column 5, lines 26-38 and 49-60; column 6, lines 19-32; and Figure 3). In regards to Eisen, the tag bits set within the sequencer are set when a cache miss occurs, thereby making it a miss tag. A person of ordinary skill in the art at the time the invention was made, and as taught by Eisen, would have recognized that the tags allow a system to start fetching instructions from the cache before the entire block has been written (Eisen column 4, lines 23-40), thereby reducing fetch delays and improving cache memory management and system performance (Eisen column 4, lines 14-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the tags of Eisen in the device of Riordan to improve cache memory management and system performance.

15. In addition, Riordan has not taught comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss and inhibiting issuance of instructions to one or more other pipelines by comparing a

destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss. Merchant has taught comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss (Merchant column 1, lines 26-50 and column 2, line 42 to column 3, line 7) and inhibiting issuance of instructions to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss (Merchant column 1, lines 26-50 and column 2, line 42 to column 3, line 7). In regards to Merchant, by not scheduling dependent instructions to execute when an instruction is dependent upon a stalled instruction, the system is effectively inhibiting the instruction from executing. A person of ordinary skill in the art at the time the invention was made, and as recognized by Merchant, would have recognized that out-of-order execution and replaying cache miss load instructions reduces overall latency (Merchant column 1, lines 39-40) and prevents incorrect data from polluting the cache system and wasting bus resources (Merchant column 3, lines 1-7), thereby increasing performance (Merchant column 1, lines 39-40) and ensuring correct data is executed on. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order execution and replay of Merchant in the device of Riordan to increase performance and ensuring correct data.

16. Referring to claim 15, Riordan has taught wherein exiting the stall state to allow one or more instructions to issue occurs after fill data is provided to a data cache (Riordan column 3, lines 11-38).

17. Referring to claims 17 and 18, Riordan has taught wherein a load miss may be present in which comparison of the tag and the fill tag identifies fill data to its corresponding load miss (Applicant's claim 18) (Riordan column 3, lines 11-38). Riordan has not explicitly taught

a. Reading the miss tag from a read queue that stores one or more load misses, wherein the miss tag identifies the load miss (Applicant's claim 17); and

b. Miss tags (Applicant's claim 18).

18. However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Eisen has taught

a. Reading the miss tag from a read queue that stores one or more load misses, wherein the miss tag identifies the load miss (Applicant's claim 17) (Eisen column 5, lines 26-38 and 49-60; column 6, lines 19-32; and Figure 3); and

b. Miss tags (Applicant's claims 18) (Eisen column 5, lines 26-38 and 49-60; column 6, lines 19-32; and Figure 3).

19. In regards to Eisen, the tag bits set within the sequencer are set when a cache miss occurs, thereby making it a miss tag. A person of ordinary skill in the art at the time the invention was made, and as taught by Eisen, would have recognized that the tags allow a system to start fetching instructions from the cache before the entire block has been written (Eisen column 4, lines 23-40), thereby reducing fetch delays and improving cache memory management and system performance (Eisen column 4, lines 14-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the tags of Eisen in the device of Riordan to improve cache memory management and system performance.

20. Referring to claim 27, Riordan has taught a computer accessible medium comprising one or more data structures to manufacture a processor, the processor including:

a. A control circuit, wherein the control circuit is configured to detect a replay of an instruction in a load/store pipeline due to a load miss (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1), and

b. Wherein the control circuit is configured to enter into a stall state and inhibit issuance of instructions to the load/store pipeline until fill data in response to the load miss is returned for loading (Riordan column 3, lines 11-38),

c. The control circuit to compare the stored tag to a fill tag that is sent to the control circuit when fill data is returned (Riordan column 3, lines 11-38). In regards to Riordan, the stored tag is the address of the instruction and the fill tag is the TAG field.

d. In which when the tag and the fill tag match, the control circuit is to exit the stall state to start issuing instructions from the queue to the pipelines (Riordan column 3, line 52 to column 4, line 2).

21. Riordan has not explicitly taught

a. A queue configured to store one or more instructions to be issued; and

b. A control circuit coupled to the queue

c. The control circuit further includes a storage device to store a miss tag corresponding to the load miss

22. However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Eisen has taught

a. A queue configured to store one or more instructions to be issued (Eisen column 2, lines 10-14; column 5, lines 37; and Figure 3); and

b. A control circuit coupled to the queue (Eisen column 5, lines 26-38 and Figure 3);

c. The control circuit further includes a storage device to store a miss tag corresponding to the load miss (Eisen column 5, lines 26-38 and 49-60; column 6, lines 19-32; and Figure 3).

23. In regards to Eisen, the tag bits set within the sequencer are set when a cache miss occurs, thereby making it a miss tag. A person of ordinary skill in the art at the time the invention was made, and as taught by Eisen, would have recognized that the tags allow a system to start fetching instructions from the cache before the entire block has been written (Eisen column 4, lines 23-40), thereby reducing fetch delays and improving cache memory management and system performance (Eisen column 4, lines 14-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the tags of Eisen in the device of Riordan to improve cache memory management and system performance.

24. In addition, Riordan has not taught inhibiting issuance of instructions to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss. Merchant has taught inhibiting issuance of instructions to one or more other pipelines by comparing a destination register corresponding to the instruction causing the load miss to other instructions in

the queue for dependencies to the load miss (Merchant column 1, lines 26-50 and column 2, line 42 to column 3, line 7). In regards to Merchant, by not scheduling dependent instructions to execute when an instruction is dependent upon a stalled instruction, the system is effectively inhibiting the instruction from executing. A person of ordinary skill in the art at the time the invention was made, and as recognized by Merchant, would have recognized that out-of-order execution and replaying cache miss load instructions reduces overall latency (Merchant column 1, lines 39-40) and prevents incorrect data from polluting the cache system and wasting bus resources (Merchant column 3, lines 1-7), thereby increasing performance (Merchant column 1, lines 39-40) and ensuring correct data is executed on. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order execution and replay of Merchant in the device of Riordan to increase performance and ensuring correct data.

25. In regards to claims 10-12 and 23-25, Riordan has not taught

a. Wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more instructions lack dependency to the load miss (Applicant's claim 10).

b. Wherein dependencies to the load miss are maintained by one or more scoreboards coupled to the control circuit (Applicant's claim 11).

c. Wherein the control circuit is configured to detect dependencies on the load miss using one or more scoreboards which track instructions that have passed a first stage of a pipeline where replay is signaled (Applicant's claim 12).

d. Permitting issuance of one of the one or more instructions if one or more instructions lack the dependency to the load miss (Applicant's claim 23).

e. Detecting lack of dependency for an instruction in one or more scoreboards (Applicant's claim 24).

f. Detecting lack of dependency for an instruction by checking one or more scoreboards which track instructions that have passed a stage of the pipeline where replay is signaled (Applicant's claim 24).

26. Merchant has taught

a. Wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more instructions lack dependency to the load miss (Applicant's claim 10) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

b. Wherein dependencies to the load miss are maintained by one or more scoreboards coupled to the control circuit (Applicant's claim 11) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

c. Wherein the control circuit is configured to detect dependencies on the load miss using one or more scoreboards which track instructions that have passed a first stage of a pipeline where replay is signaled (Applicant's claim 12) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

d. Permitting issuance of one of the one or more instructions if one or more instructions lack the dependency to the load miss (Applicant's claim 23) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

e. Detecting lack of dependency for an instruction in one or more scoreboards (Applicant's claim 24) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

f. Detecting lack of dependency for an instruction by checking one or more scoreboards which track instructions that have passed a stage of the pipeline where replay is signaled (Applicant's claim 24) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

27. A person of ordinary skill in the art at the time the invention was made, and as recognized by Merchant, would have recognized that out-of-order execution and replaying cache miss load instructions reduces overall latency (Merchant column 1, lines 39-40) and prevents incorrect data from polluting the cache system and wasting bus resources (Merchant column 3, lines 1-7), thereby increasing performance (Merchant column 1, lines 39-40) and ensuring correct data is executed on. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order execution and replay of Merchant in the device of Riordan to increase performance and ensuring correct data.

Response to Arguments

28. Applicant's arguments with respect to claims 1-2, 4-5, 10-12, 14-15, 17-18, 23-25, and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
10 November 2005

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